MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 1, 2019/2020

EEN1046 – ELECTRONICS III

(TE, RE)

19 OCTOBER 2019
2.30 p.m. – 4.30 p.m.
(2 Hours)

INSTRUCTIONS TO STUDENT

1. This booklet consists of 8 pages including cover pages with 4 questions only.
2. Attempt **ALL** questions given. All questions carry equal marks and distribution of the marks for each question is given.
3. Please write all your answers in the Answer Booklet provided.
4. All necessary working **MUST** be shown.

Question 1

(a) Derive the equation for the output voltage, V_O of the amplifier circuit as shown in Figure Q1 (a). Based on the equation that you have derived, identify the mathematical operation of this op amp circuit. Assume ideal op-amp.

[7 marks]

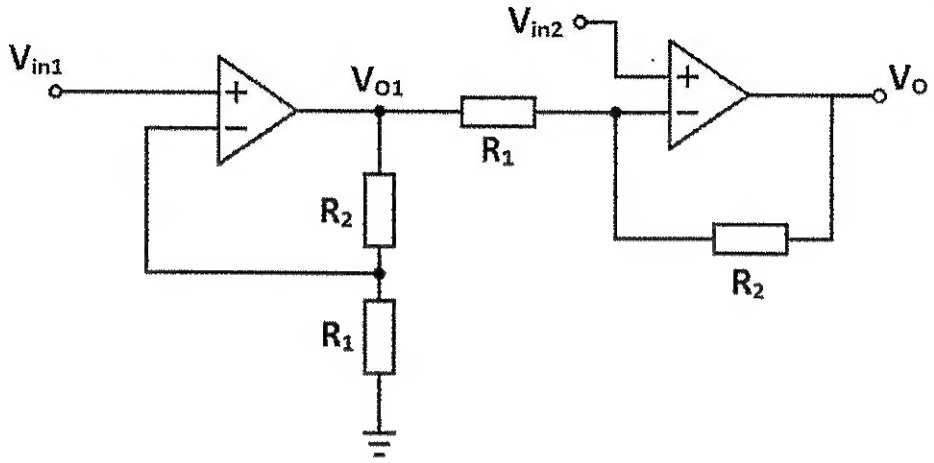

Figure Q1 (a)

(b) Determine the input voltage and output voltage for the circuit as shown in Figure Q1 (b). Assume ideal op-amp.

[5 marks]

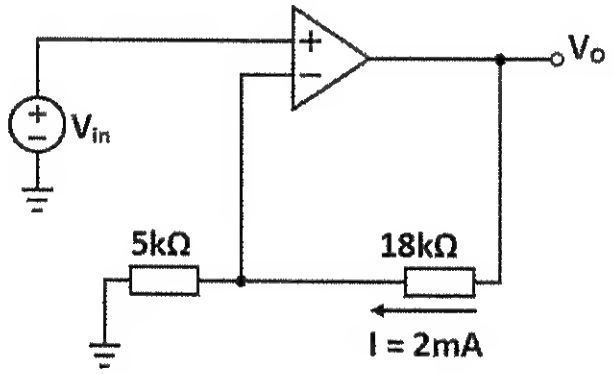

Figure Q1 (b)

(c) Refer to the ideal op amp circuit as shown in Figure Q1(c), given that R = 10kΩ, R_L = 5kΩ, V_1 = 5V and V_2 = 1V.

(i) Derive the equation of I_L in terms of input voltages.

[7 marks]

(ii) Find the values of I_L and V_L.

[4 marks]

(iii) Calculate the output voltage, V_O.

[2 marks]

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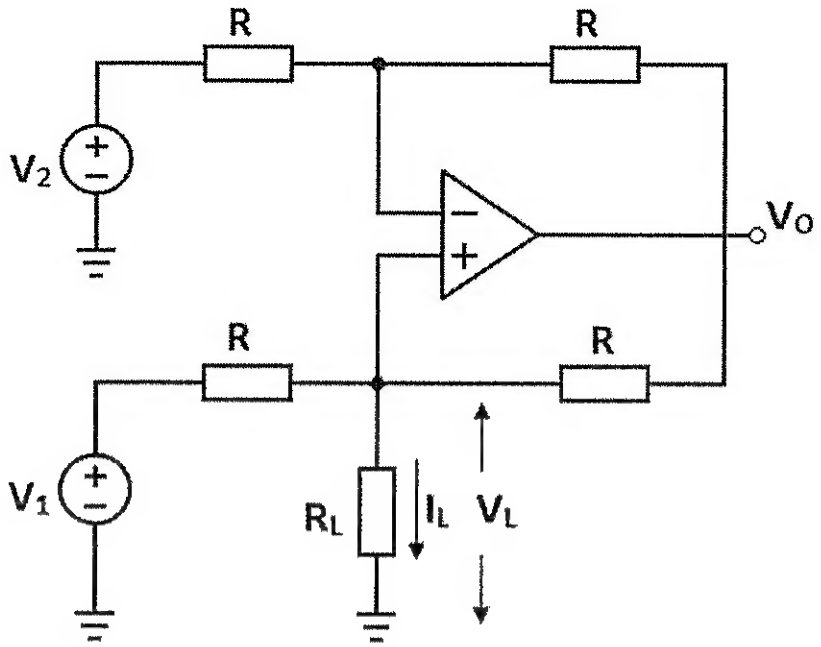

Figure Q1 (c)

Question 2

(a) A voltage regulator circuit is shown in Figure Q2 (a). Assume ideal op-amp and other values are; R=1 KΩ, R_1 = 40k Ω, R_2=20 kΩ, V_Z=3 V, V_{BE} = 0.7 V and unregulated power supply=15 V.

(i) Identify the type of the regulator circuit.

[1 mark]

(ii) Determine the regulated output voltage V_O.

[2 marks]

(iii) How the output voltage remains constant at the calculated value in part (ii) if the unregulated power supply decreases?

[4 marks]

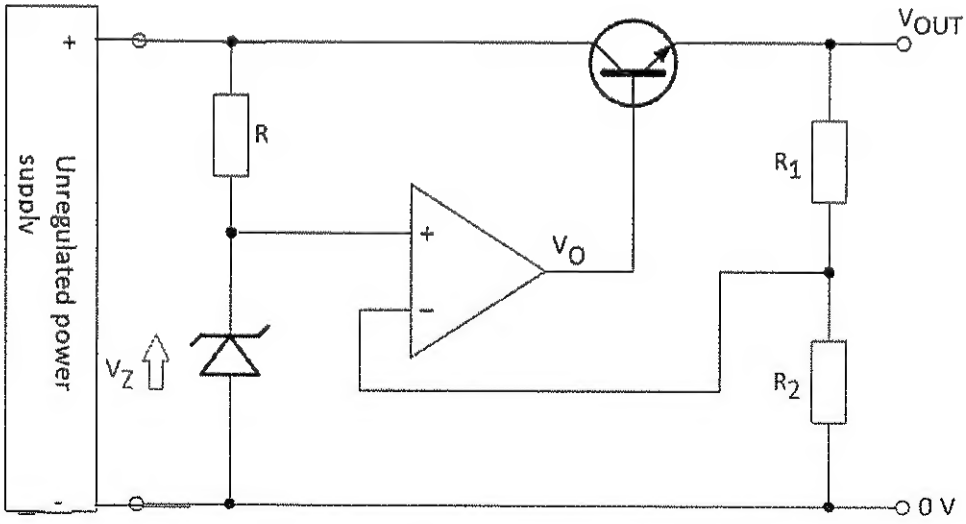

Figure Q2 (a)

Continued ...

(b) An oscillator circuit is shown in Figure Q2 (b).

(i) Identify the type of oscillator circuit.

[1 mark]

(ii) What is the purpose of introducing 3 RC networks in the output terminal?

[2 marks]

(iii) Design the circuit to get the oscillating frequency of 2kHz. Take R_1=1kΩ.

[3 marks]

(iv) How the circuit can achieve amplitude stabilization? Explain with proper circuit diagram.

[4 marks]

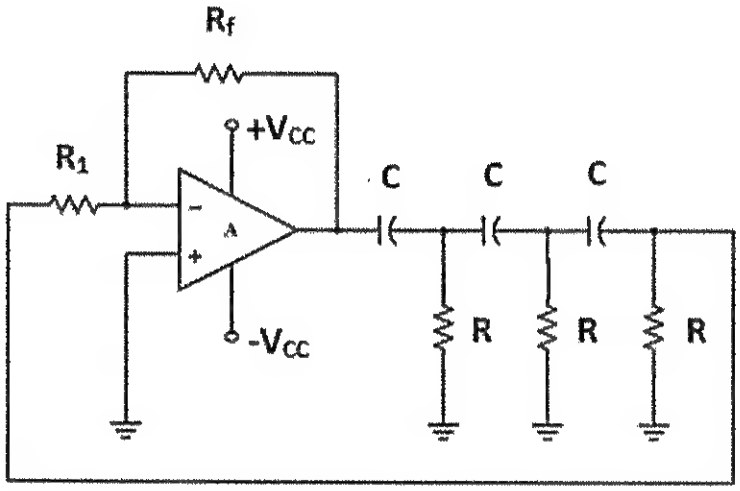

Figure Q2 (b)

(c) Figure Q2 (c) shows a Band-Pass filter circuit with constant pass-band gains. Given R_1=R_1'=R_F=R_F'=10kΩ, C=10nF, R=10kΩ, C'=5nF, R'=12kΩ and Bandwidth, BW =1k Hz.

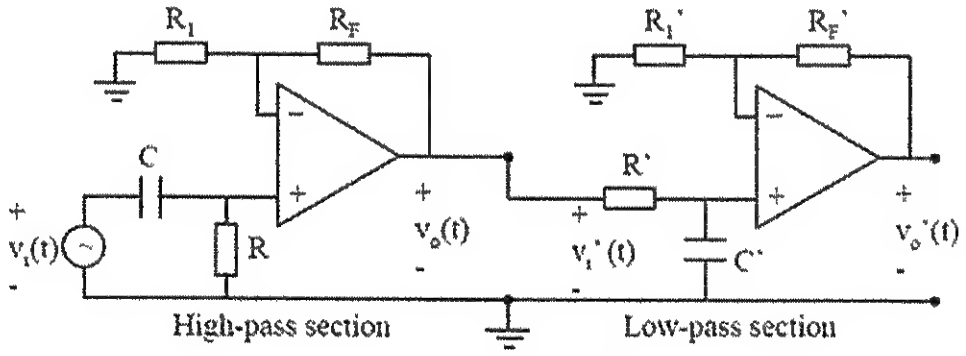

Figure Q2 (c)

(i) Calculate the high pass gain, K_{HP} and low pass gain, K_{LP}.

[2 marks]

(ii) Calculate the overall band pass gain, K_{BP}.

[2 marks]

Continued ...

(iii) Calculate the higher cutoff frequency, f_H and lower cutoff frequency, f_L.

[2 marks]

(iv) Calculate the quality factor Q.

[2 marks]

Question 3

A non-ideal op-amp as shown in Figure Q3 is internally compensated such that open loop roll off is -20dB/decade in Bode plot. The open loop gain at 10kHz was measured to be 40dB. The slew rate is 2V/μs and the saturation limits are ±14V. The input bias currents and the input offset voltage are 10nA, and 1mV.

(a) Determine the unity gain bandwidth of the op amp.

[4 marks]

(b) Find the full power bandwidth of the circuit.

[4 marks]

(c) Find the output offset voltage when the input voltage is 0V. Given that $R_F = 98k\Omega$, $R_1 = 2k\Omega$ and $R_C = 10k\Omega$.

[11 marks]

(d) If the op amp is treated ideally, what will happen to the answers in (b) and (c)? Justify your answers.

[6 marks]

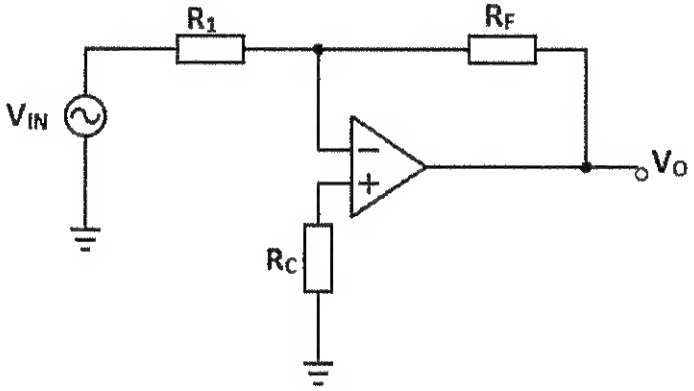

Figure Q3

Continued ...

Question 4

(a) What are the basic differences between op-amp and comparator?

[2 marks]

(b) Design an inverting configuration for non-inverting threshold comparator whose transfer characteristic is shown in Figure Q4 (b). Also sketch the circuit. Take V_R=2 V, V_{ref}=2.5 V.

[7 marks]

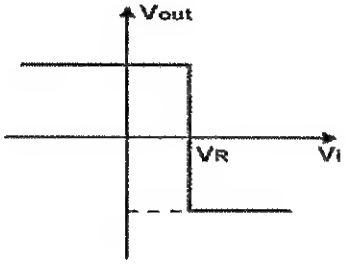

Figure Q4 (b)

(c) Sketch the output wave form of the circuit as shown in Figure Q4 (c) when input signal is sinusoidal wave. Consider ideal op-amp.

[2 marks]

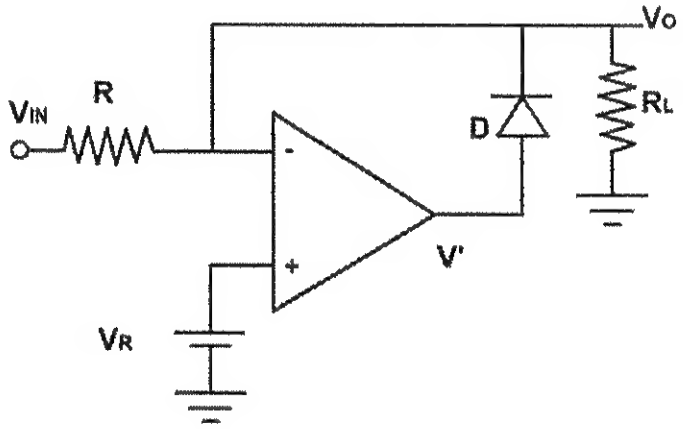

Figure Q4 (c)

(d) An improved version of precision half-wave rectifier circuit is shown in Figure Q4 (d). Assume ideal op-amp. Discuss briefly, why diode D_2 is included in the circuit? Also draw the transfer characteristics of the circuit.

[4 marks]

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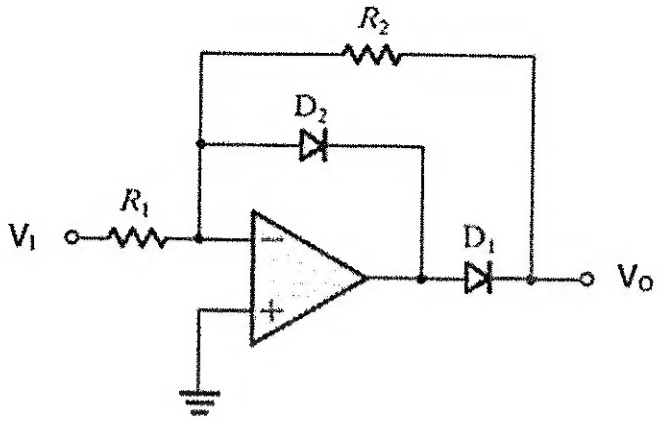

Figure Q4 (d)

(e) Evaluate the output of the circuit shown in Figure Q4 (e) when a sinusoidal input V_i=10 Sinωt is applied to the circuit. Also discuss briefly, how the circuit works? Assume ideal op-amps.

[6 marks]

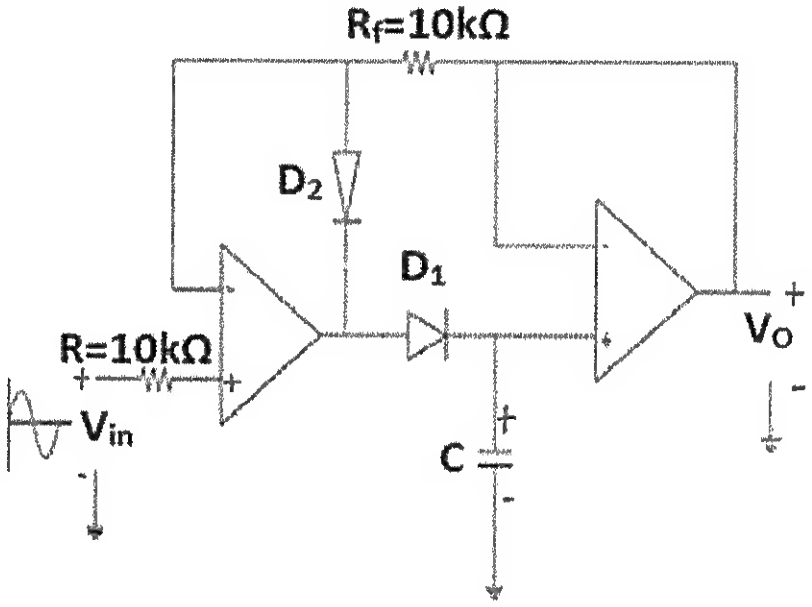

Figure Q4 (e)

(f) Evaluate the voltages Va and Vb in the circuit of Figure Q4 (f). For the transistor it is given that; $V_{BE}=-k_1\log[V_{in}/K_2]$ where K_1 and K_2 are constants. Assume ideal op-amps. Take, $R_1=R_2=R_6$ and $R_3=R_4=R_5$ and $R_7=R_8$. The voltage gain of an op-amp "a" is $-K_2$. Show all the steps clearly.

[4 marks]

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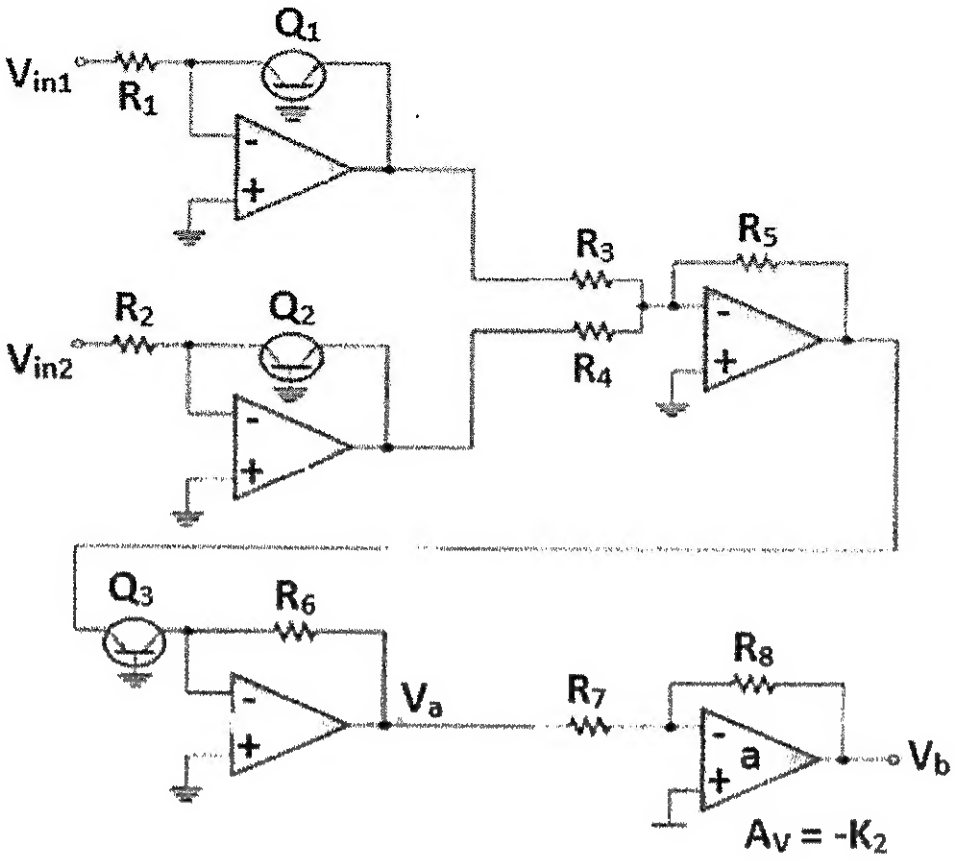

Figure Q4 (f)

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